# ABSTRACT

Low density parity-check (LDPC) codes are known to have excellent performance for high speed data transmission and low complexity. However, moderate-length or short length binary LDPC codes have been shown to have an early error floor and degraded decoding performance. They had been adopted as part of a number of standards such as Wi-Max (IEEE 802.16). In high speed applications, parallel implementations of iterative message-passing algorithms for the decoding of LDPC codes are preferred. To reduce the complexity of the algorithm, which translates to reducing the area and power consumption as well as increasing the throughput, researchers have used min-sum (MS) algorithm. LDPC codes are suitable for iterative decoding, i.e. an iterative decoder can perform successive decoding of both rows and column. LDPC implements parallelism in the decoding process thereby achieving high decoding throughput. Even though performance is reduced, the hardware complexity of the Belief Propagation( BP) algorithm can be significantly minimized, by replacing complex computations of check nodes with simple summation and comparison operations, which significantly reduces the latency and hardware complexity. The min-sum algorithm does not require channel information like noise variance for additive white Gaussian noise (AWGN) channel and provide less sensitive decoding performance under finite word-length implementations over the BP algorithm. Due to this advantage, MS algorithm is widely used in LDPC decoders for low power consumption.

Considering the above facts, the proposed work uses min-sum (MS) algorithm and focuses on low complexity design of LDPC hardware architecture by replacing complex computations of check nodes with simple summation and comparison operations, which significantly reduces the latency and hardware complexity. The parameters considered for

investigation include hardware utilization parameter such as gate counts, memory usage, power and current consumption.

The proposed method of LDPC decoder design comprises of several processing elements— variable node unit (VNU), check node unit (CNU), address generator, minimum data generator and Euclidean orthogonal generator.The interconnections between CNUs and VNUs are provided by the routing networks. The connectivity provided by the parity-check matrix creates the label for input and output edges of the CNU. After the completion of required number of iterations, the VNU produces the final outputs. The minimum data generator unit selects the minimum decoded value from variable node unit to generate the decoding sequence. Euclidean orthogonal generator is used to determine the level of noise on the received signal. The output from CNU is fed into the Euclidean orthogonal generator, which consists of Adder/Subtractor, shifter and multiplexers. It produces the real and imaginary part of the received signal from CNU. If the real term is greater than the imaginary term, then the signal from CNU is passed through the VNU in order to decode the signals, else it is discarded due to the high severity of noise on the received sequences.

The proposed low power LDPC decoder is used to superimpose and deimpose the received signal into unicast and broadcast signals for Orthogonal Frequency Division Multiplexing(OFDM) signal transmission and reception. The decoded signal from LDPC decoder is passed through Fast Fourier Transform(FFT) architecture in order to convert the time domain signal into frequency domain signal. The broadcast decoded signal streams are demodulated using higher order modulation Quadrature Phase Shift Keying(QPSK) and unicast decoded signal streams are demodulated using lower order Modulation Binary Phase Shift Keying(BPSK).This proposed

architecture is tested on different Complex Programmable Logic Device(CPLD) processor for analyzing its power consumption.

The Modelsim 5.8 is used to simulate and evaluate the proposed method. Intel Pentium Core i3 machine 2.4 GHz with 2GB of internal RAM is used in this research. The designed architecture consumes 0.031mW of power with an operating frequency of 100MHz at the maximum. The proposed architecture consumes 4-input LUTs of about 100, which provides a low hardware complexity compared to the conventional LDPC architecture. The decoding latency obtained for both check node and variable node implementations in the proposed architecture is about 22.02ns.The proposed LDPC and their hardware architecture are designed and tested on various versions of Spartan-3E, Virtex and CPLD family device using Xilinx 9.2i Project Navigator.The main application of the proposed LDPC decoder is to decode the multi user signals efficiently from the fading channels.